Amendments to the Drawings

See Attached Drawings

FIG. 1

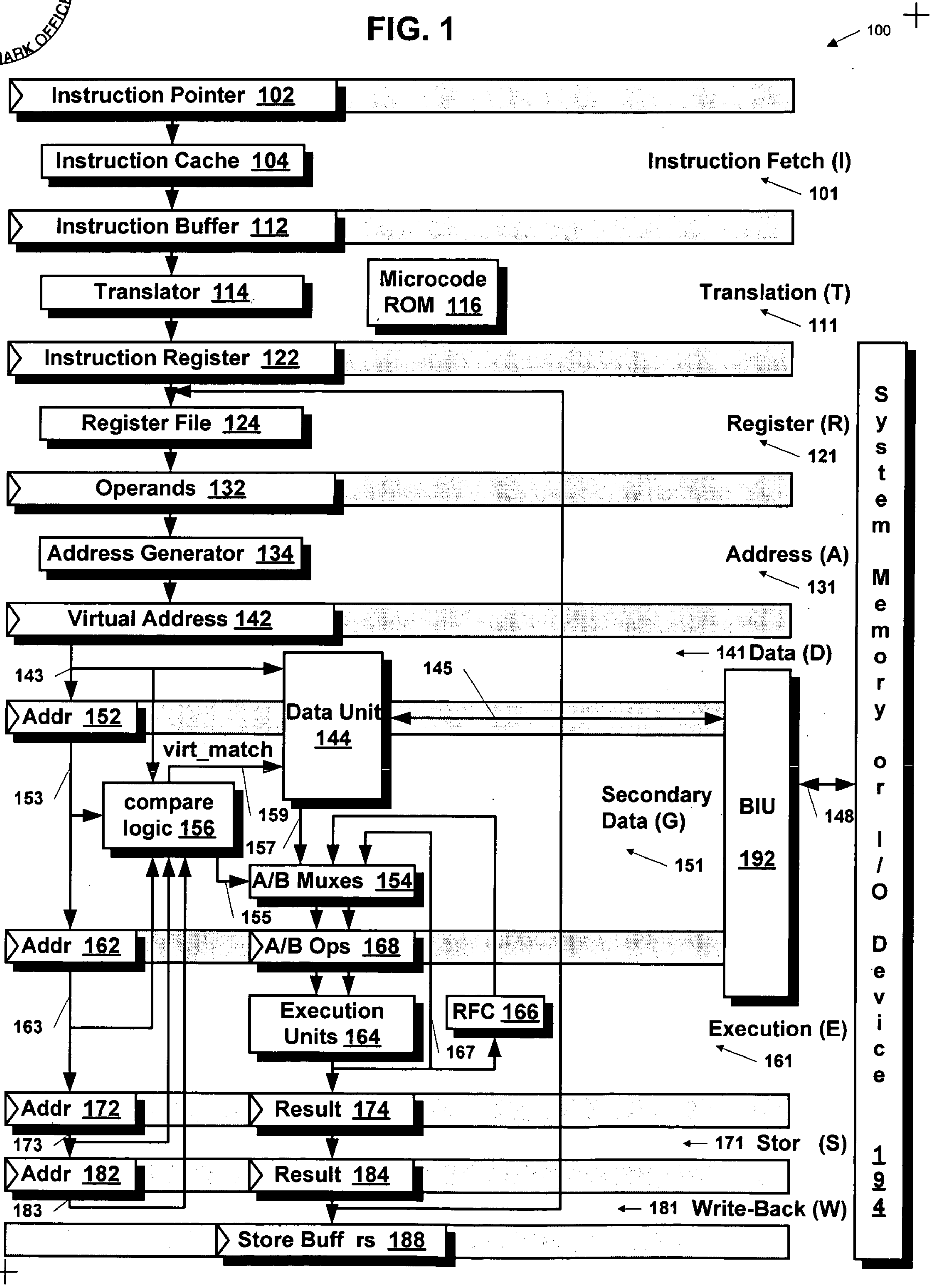
100
Instruction Pointer 102
Instruction Cache 104
Instruction Fetch (I)
101
Instruction Buffer 112
Translator 114
Microcode ROM 116
Translation (T)
111
Instruction Register 122
Register File 124
Register (R)
121
Operands 132
Address Generator 134
Address (A)
131
Virtual Address 142
141 Data (D)
143
145
Addr 152
Data Unit 144
virt_match
153
compare logic 156
159
157
Secondary Data (G)
151
BIU 192
148
A/B Muxes 154
155
Addr 162
A/B Ops 168
Execution Units 164
RFC 166
167
163
Execution (E)
161
Addr 172
Result 174
173
171 Stor (S)
Addr 182
Result 184
183
181 Write-Back (W)
Store Buff rs 188
System Memory or I/O Device 194

FIG. 2

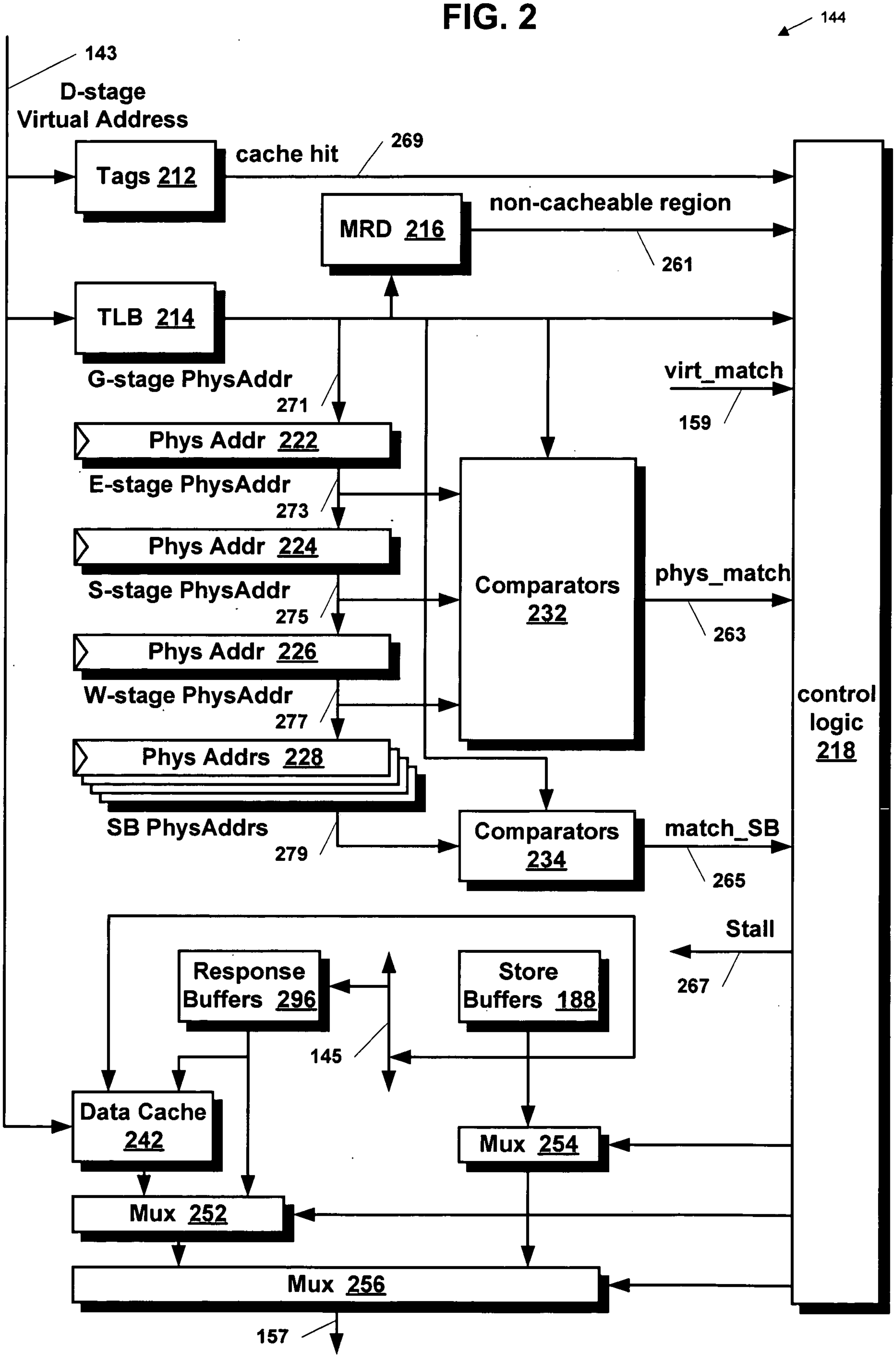
144
143
D-stage
Virtual Address
Tags 212
cache hit
269
MRD 216
non-cacheable region
261
TLB 214
G-stage PhysAddr
271
virt_match
159
Phys Addr 222
E-stage PhysAddr
273
Phys Addr 224
S-stage PhysAddr
275
Comparators
232
phys_match
263
Phys Addr 226
W-stage PhysAddr
277
control
logic
218
Phys Addrs 228
SB PhysAddrs
279
Comparators
234
match_SB
265
Stall
267
Response
Buffers 296
Store
Buffers 188
145
Data Cache
242
Mux 254
Mux 252
Mux 256
157

FIG. 3

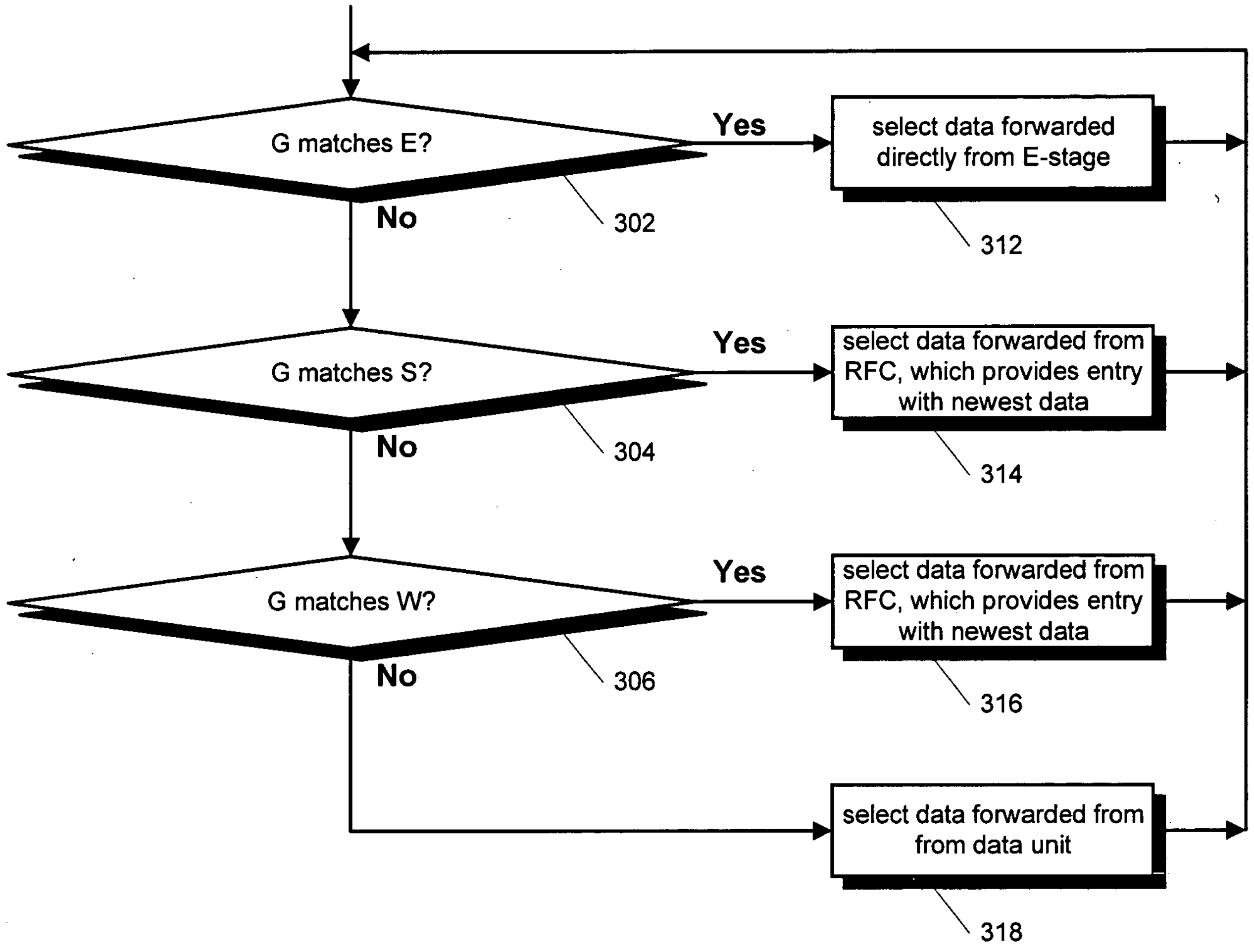
G matches E?
Yes
select data forwarded directly from E-stage
No
302
312
G matches S?
Yes
select data forwarded from RFC, which provides entry with newest data
No
304
314
G matches W?
Yes
select data forwarded from RFC, which provides entry with newest data
No
306
316
select data forwarded from from data unit
318

FIG. 4

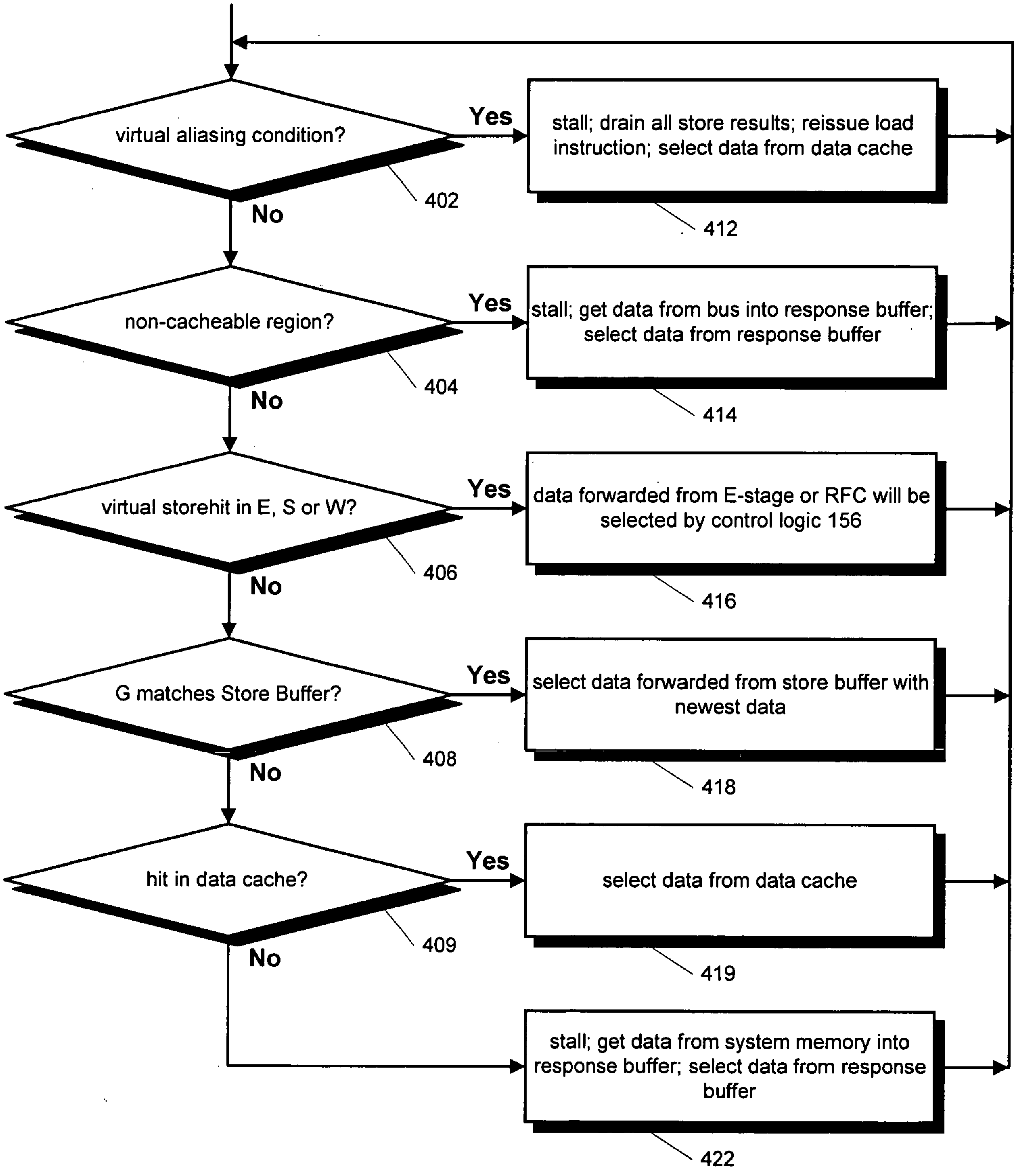
virtual aliasing condition?
Yes
stall; drain all store results; reissue load instruction; select data from data cache
402
No
412
non-cacheable region?
Yes
stall; get data from bus into response buffer; select data from response buffer
404
No
414
virtual storehit in E, S or W?
Yes
data forwarded from E-stage or RFC will be selected by control logic 156
406
No
416
G matches Store Buffer?
Yes
select data forwarded from store buffer with newest data
408
No
418
hit in data cache?
Yes
select data from data cache
409
No
419
stall; get data from system memory into response buffer; select data from response buffer
422

FIG. 5

Forwarding from RFC

Cycle	Address (A)	Data (D)	Sec'y Data (G)	Execution (E)	Store (S)	Write-back (WB)	Store Buffers (SB)
1	st [MA1], R2						
2	nop	st [MA1], R2					
3	ld R3, [MA1]	nop	st [MA1], R2				
4		ld R3, [MA1]	nop	st [MA1], R2			
5			ld R3, [MA1]	nop	st [MA1], R2		
6				ld R3, [MA1]	nop	st [MA1], R2	
7					ld R3, [MA1]	nop	st [MA1], R2
8						ld R3, [MA1]	

Note: The load/store instructions specify the same virtual load/store address.
Clock 4, E-stage: Result data destined for memory also written into RFC.
Clock 5, G-stage: Result data specified by load instruction forwarded from RFC.

FIG. 6

Forwarding from Store Buffer

Cycle	Address (A)	Data (D)	Sec'y Data (G)	Execution (E)	Store (S)	Write-back (WB)	Stor Buff rs (SB)
1	st [MA1], R2						
2	st [MA1], R3	st [MA1], R2					
3	add R4, R5, R4	st [MA1], R3	st [MA1], R2				
4	add R7, R8, R7	add R4, R5, R4	st [MA1], R3	st [MA1], R2			
5	sub R4, R5, R4	add R7, R8, R7	add R4, R5, R4	st [MA1], R3	st [MA1], R2		
6	sub R7, R8, R7	sub R4, R5, R4	add R7, R8, R7	add R4, R5, R4	st [MA1], R3	st [MA1], R2	
7	ld R9, [MA1]	sub R7, R8, R7	sub R4, R5, R4	add R7, R8, R7	add R4, R5, R4	st [MA1], R3	st [MA1], R2
8		ld R9, [MA1]	sub R7, R8, R7	sub R4, R5, R4	add R7, R8, R7	add R4, R5, R4	st [MA1], R3
9			ld R9, [MA1]	sub R7, R8, R7	sub R4, R5, R4	add R7, R8, R7	
10				ld R9, [MA1]	sub R7, R8, R7	sub R4, R5, R4	
11					ld R9, [MA1]	sub R7, R8, R7	
12						ld R9, [MA1]	

Note: The load/store instructions specify the same load/store address.
Clock 7, E-stage: Result data of first store instruction from R2 destined for memory written into first store buffer.
Clock 8, E-stage: Result data of second store instruction from R3 destined for memory written into second store buffer.
Clock 9, G-stage: Result data specified by load instruction forwarded from second store buffer.

FIG. 7

Speculative Forwarding with Correction Due to Virtual Aliasing Condition

Cycle	Address (A)	Data (D)	Sec'y Data (G)	Execution (E)	Store (S)	Write-back (WB)	Store Buffers (SB)
1	st [MA1], R2						
2	ld R4, [MA2]	st [MA1], R2					
3		ld R4, [MA2]	st [MA1], R2				
4			ld R4, [MA2]	st [MA1], R2			
5				ld R4, [MA2]	st [MA1], R2		
6				ld R4, [MA2]		st [MA1], R2	
7				ld R4, [MA2]			st [MA1], R2
n-1				ld R4, [MA2]			
n		ld R4, [MA2]					
n+1			ld R4, [MA2]				
n+2				ld R4, [MA2]			
n+3					ld R4, [MA2]		
n+4						ld R4, [MA2]	

Note: The load/store instructions specify different virtual load/store addresses that translate to the same physical address.
Clock 5, E-stage: Data from data unit speculatively forwarded to E-stage load instruction.
Clocks 5 through n-1, E-stage: Load instruction in stalled E-stage while store instruction data written to data cache.
Clock 7, Store Buffers: Result data of store instruction destined for memory written into store buffer.
Clock n, D-stage: Load instruction reissued within data unit.
Clock n+1, G-stage: Load instruction generates hit in data cache.

FIG. 8

Speculative Forwarding with Correction Due to Access of Non-Cacheable Region

Cycle	Address (A)	Data (D)	Sec'y Data (G)	Execution (E)	Store (S)	Write-back (WB)	Stor Buff rs (SB)
1	st [MA1], R2						
2	nop	st [MA1], R2					
3	ld R3, [MA1]	nop	st [MA1], R2				
4		ld R3, [MA1]	nop	st [MA1], R2			
5			ld R3, [MA1]	nop	st [MA1], R2		
6				ld R3, [MA1]	nop	st [MA1], R2	
7				ld R3, [MA1]		nop	st [MA1], R2
n-1				ld R3, [MA1]			
n				ld R3, [MA1]			
n+1					ld R3, [MA1]		
n+2						ld R3, [MA1]	

Note: The load/store instructions specify the same virtual load/store address which translates to a physical address in a non-cacheable region.

Clock 6, E-stage: Storehit data from RFC speculatively forwarded to E-stage load instruction.

Clocks 6 through n-1, E-stage: Load instruction stalled in E-stage while data specified by load instruction is fetched from I/O device or system memory into a response buffer.

Clock n, E-stage: Data requested by load instruction selected from response buffer.